

MIXED-MODE HARDWARE MULTITHREADING**BACKGROUND OF THE INVENTION****1. Technical Field:**

The present invention relates to an improved data
5 processing system and, more particularly, to hardware
multithreading.

2. Description of Related Art:

The operating system (OS) software controlling most
modern computers enables multitasking. That is, it
10 enables multiple tasks (programs, threads, or processes)
to be executed concurrently. On single-processor
systems, task execution of multiple programs is typically
interleaved to give the appearance of concurrency,
whereas on symmetric multiprocessors, a single operating
15 system distributes the various tasks over multiple
processors. Even in a symmetric multiprocessor (SMP),
the number of tasks can outnumber the number of
processors such that multiple tasks must be interleaved
on a single processor to give the appearance of
20 concurrency.

Task interleaving under control of the operating
system is sometimes referred to as coarse-grain
multithreading. Because all the user-level resources
must be available to each task, the operating system must
25 save the user-state of a task, such as the values in the
registers, to memory, and restore the state of a second
task whose execution is to be resumed, on every task
switch. When multiple tasks execute on a single
processor, the decision to switch tasks is commonly made

Docket No. AUS920000649US1

on the basis of either a timer interrupt (this is called "time-slicing") or the execution of an operation that is visible to the operating system, such as I/O or a translation miss, by the task that is running.

5 On a multithreaded processor, the state of more than one thread is available in the registers of the processor. This has the advantage that a task switch can occur without requiring all the state in the processor's architectural registers to be saved in memory first, and
10 hence a thread switch can occur with little overhead. Three types of hardware multithreaded processors are known.

1.) Interleaved multithreaded processors, such as used in the TERA computer. In this case, in cycle n ,
15 instructions from thread $n \bmod m$, where m is the number of simultaneously executing threads, are issued.

2.) Hardware multithreaded processors, such as the IBM Northstar AS-400 series processor. In this processor the hardware switches between two threads based on
20 lower-level events, such as a cache miss.

3.) Simultaneous multithreading, in which instructions from multiple threads are issued in the same cycle.

Method 1.) has the disadvantage that issue slots go
25 unused if one of the threads is idle. Method 2.) has the disadvantage that issue slots are poorly utilized by a single thread because of dependencies between instructions. This disadvantage is especially significant in deeply pipelined processors. Method 3.)
30 has the disadvantage that all registers of all threads must be accessible at all times, hence register files in SMT architectures tend to be large and slow.

Docket No. AUS920000649US1

It would therefore be desirable to have a new type of mixed-mode multithreading that does not suffer from these disadvantages.

SUMMARY OF THE INVENTION

The present invention provides a mixed-mode multithreading processor. In one embodiment, the multi-mode multithreading processor includes a multithreaded register file with a plurality of registers, a thread control unit, and a plurality of hold latches. Each of the hold latches and registers stores data representing a first instruction thread and a second instruction thread. The thread control unit provides thread control signals to each of the hold latches and registers selecting a thread using the data. The thread control unit provides control signals for interleaving multithreading except when a long latency operation is detected in one of the threads. During a predetermined period corresponding approximately to the duration of the long latency operation, the thread control unit places the processor in a mode in which only instructions corresponding to the other thread are read out of the hold latches and registers. Once the predetermined period of time has expired, the processor returns to interleaving multithreading.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, further objectives and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 depicts a block diagram of a data processing system in which the present invention may be implemented in accordance with a preferred embodiment of the present invention;

Figure 2 depicts a block diagram of a basic reduced instruction set chip (RISC) processor in accordance with the present invention;

Figure 3 depicts a block diagram of a thread control system in accordance with the present invention;

Figure 4 depicts a flowchart illustrating an exemplary process for selecting multithreading modes for a state holding register in accordance with the present invention; and

Figure 5 depicts a flowchart illustrating an exemplary control for a state holding register.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to **Figure 1**, a block diagram of a data processing system in which the present invention may be implemented is depicted in accordance with a preferred embodiment of the present invention. Data processing system **100** may be a symmetric multiprocessor (SMP) system including a plurality of processors **102** and **104** connected to system bus **106**. Alternatively, a single processor system may be employed. Also connected to system bus **106** is memory controller/cache **108**, which provides an interface to local memory **109**. I/O bus bridge **110** is connected to system bus **106** and provides an interface to I/O bus **112**. Memory controller/cache **108** and I/O bus bridge **110** may be integrated as depicted.

Peripheral component interconnect (PCI) bus bridge **114** connected to I/O bus **112** provides an interface to PCI local bus **116**. A number of modems may be connected to PCI bus **116**. Typical PCI bus implementations will support multiple PCI expansion slots or add-in connectors.

Communications links to network computers **108-112** in **Figure 1** may be provided through modem **118** and network adapter **120** connected to PCI local bus **116** through add-in boards.

Additional PCI bus bridges **122** and **124** provide interfaces for additional PCI buses **126** and **128**, from which additional modems or network adapters may be supported. In this manner, data processing system **100** allows connections to multiple network computers. A memory-mapped graphics adapter **130** and hard disk **132** may also be connected to I/O bus **112** as depicted, either

directly or indirectly.

Each of processors **102** and **104** supports multithreading. Multithreading is multitasking within a single program.

5 Certain types of applications lend themselves to multithreading. For example, in an order processing system, each order can be entered independently of the other orders. In an image editing program, a calculation-intensive filter can be performed on one
10 image, while the user works on another. In a symmetric multiprocessing (SMP) operating system as depicted, its multithreading allows multiple processors **102** and **104** to be controlled at the same time. Multithreading is also used to create synchronized audio and video applications.

15 To allow multithreading on each processor **102** and **104**, each processor **102** and **104** contains a plurality of latches as will be recognized by one skilled in the art. The latches within the processors **102** and **104** are of two types: flow-through and hold state. Flow-through latches
20 are latches that are used to break multiple-cycle paths into distinct stages, but in which the same data is not held for multiple cycles, and are implemented unchanged from the prior art. Hold state latches are latches that store bits of data until needed by other components within
25 the processor. The hold state latches in the present invention are modified from the prior art to store two bits rather than one bit with select signals corresponding to the thread determining which state is read.

Those of ordinary skill in the art will appreciate
30 that the hardware depicted in **Figure 1** may vary. For example, other peripheral devices, such as optical disk drives and the like, also may be used in addition to or in

place of the hardware depicted. The depicted example is not meant to imply architectural limitations with respect to the present invention.

The data processing system depicted in **Figure 1** may
5 be, for example, an IBM RISC/System 6000 system, a product of International Business Machines Corporation in Armonk, New York, running the Advanced Interactive Executive (AIX) operating system.

With reference now to **Figure 2**, a block diagram of a
10 basic reduced instruction set chip (RISC) processor is depicted in accordance with the present invention. Processor **200** may be implemented as, for example, either of processors **102** and **104** in **Figure 1**. Processor **200** is an example of a processor capable of dual mode
15 multithreading (i.e. both "TERA Computer" and "AS/400 Star Series" type multithreading). "TERA Computer" multithreading mode is a type of multithreading in which instructions from the different threads strictly alternate. "AS/400 Star Series" type multithreading is a
20 type of multithreading in which a thread switch occurs in response to a long latency period, such as, for example, a load instruction that misses in the datacache.

Processor **200** includes a fetch unit **208** which
retrieves and loads instructions to be executed by
25 processor **200** from instruction cache **202**. Instruction cache **202** holds instructions from both threads executed by processor **200**. Branch unit **210** allows instructions to be fetched in advance in response to receipt of a special branch instruction. Issue and decode unit **204** interprets
30 and implements instructions received from instruction cache **202**. Data cache **212** stores data corresponding to both threads received from load/store unit **214** which loads

Docket No. AUS920000649US1

data into processor **200**.

Multithread register file **206** contains multiple registers that each hold architectural states from both threads. Execution unit A **218** and execution unit B **220**
5 execute the microcode instructions for the appropriate thread read out of multithread register file **206** and appropriate hold latches (not shown) based on thread control signals from the thread control unit **216**.

Thread control unit **216** controls the active signals
10 for the different threads depending on whether a long-latency operation has occurred in that thread. Thus, if a long latency occurs in one thread, the thread selection signals for that thread can be set to inactive and the mode of operation switched to execute only the
15 instructions for the other thread until a period of time has elapsed sufficient that the inactive thread is ready to continue. This period of time may be a predetermined predicted period of time based on the type of operation causing the latency. This predetermined period of time is
20 the time predicted to be sufficient to allow the operation that has resulted in the latency to complete. The thread selection signals flow through the pipeline with the instruction and are typically applied to the latches delayed by one or multiple cycles from the control signal
25 applied to the register file.

It should be noted that processor **200** is given merely as an example and not as an architectural limitation. For example, processor **200** may include more execution units that depicted in **Figure 2**.

30 With reference now to **Figure 3**, a block diagram of a thread control system is depicted in accordance with the present invention. Thread control system **300** may be

Docket No. AUS920000649US1

implemented in a processor, such as, processor **200** in **Figure 2**, that is capable of both "TERA Computer" and "AS/400 Star Series" type multithreading. As discussed above, "TERA Computer" multithreading mode is a type of multithreading in which instructions from the different threads strictly alternate. "AS/400 Star Series" type multithreading is a type of multithreading in which a thread switch occurs in response to a long latency period, such as, for example, a load instruction that misses in the datacache. Thread control system **300** combines both types of multithreading to gain a performance advantage in data processing systems at a minimal design and area penalty.

Thread control system **300** includes a thread control unit **302**, a plurality of hold state latches **306**, and a plurality of flow through latches **304** as well as other components not shown for simplicity. Flow through latches **304** each contain an input for data in signals **310** and an output for data out signals **312** originating and ending in other components (not shown) within the data processing system. Flow through latches **304** perform in the same fashion as flow through latches in prior art processors and are not required to be modified in any manner from the prior art. Hold state latches **306**, however, are modified from the prior art. In the prior art, the hold state latches store a single bit. In the present invention, hold state latches **306** store two bits. Thus, hold state latches **306** include two data inputs for receiving thread one data in signals **314** and thread two data in signals **316** and also includes an output for data out signals **318**. Hold state latches **306** also include a control input for

Docket No. AUS920000649US1

receiving thread control signals **308** from thread control unit **302**.

Thread control signals **308** determine which of the two state stored in hold state latches **306** are output as data out **318** from hold state latches **306**. When the processor is operating in interleaved mode (i.e. "TERA Computer" type multithreading), thread control signals **308** strictly alternate, allowing first thread one and then thread two signals to be processed. This strict alternation allows signals to be computed multiple cycles in advance, hence all cycles are utilized.

When a long latency operation, such as a load instruction that misses in the data cache or a mispredicted branch, in one of the threads is detected by thread control unit **302**, thread control unit **302** responds by skipping the control signals corresponding to that thread for a number of cycles determined by the predicted latency of the operation that is detected. Thus, during a long latency, thread control system **300** is switched from "TERA Computer" type multithreading to "AS/400 Star Series" type multithreading, thereby gaining a performance advantage over prior art processors. The cost of implementing the multithreading processor according to the present invention is much smaller than simultaneous multithreading (SMT) approaches that dynamically assign issue slots to the participating threads. Every clock cycle in the processor corresponds to an instruction issue slot and multiple instructions may be issued in a single cycle.

With reference now to **Figure 4**, a flowchart illustrating an exemplary process for selecting multithreading modes for a processor, such as, for

Docket No. AUS920000649US1

example, processor **102** or **104** in **Figure 1**, is depicted in accordance with the present invention. The present process may be implemented in, for example, thread control unit **302** in **Figure 3**. To begin, the thread

5 control unit sends signals to each hold latch to read the data bit corresponding to the first thread (step **402**).

The thread control unit then sends control signals to the hold latches to read the data bit for the second thread (step **404**). During this process of reading first one and

10 then the other thread, the thread control unit determines whether a long latency in data bits has occurred for one of the other threads (step **406**). If no latency has occurred, then the control unit continues in interleaving mode (step **414**) by returning to step **402**.

15 If a long latency has occurred in the data bits of one of the threads, then the thread control unit sends control signals to the hold latches to read the data bits out of the thread not experiencing a latency (step **408**). This continues until the thread control unit determines

20 that the expected latency period has expired (step **410**). The expected latency period may be determined, for example, by determining the type of operation that is currently being implemented in the thread with a predetermined expected value for the time necessary to

25 complete that type of operation. Once the latency period has expired and no power off event has occurred (step **412**), the thread control unit returns to interleaving mode (step **414**). It is important to note that in a pipelined implementation, that the alternating selection

30 of the register bit should be synchronized with the instruction issued.

With reference now to **Figure 5**, a flowchart illustrating an exemplary control for a state holding register is depicted in accordance with the present invention. To begin, a thread control unit determines
5 whether both threads 0 and 1 are active (step **502**). Initially, control signals for both threads are set to active and are set to inactive for a predetermined amount of time on a long-latency operation with the predetermined amount of time depending on the type of
10 operation detected. Thus, if both threads 0 and 1 are active, the latch is instructed to read (or write as the case may be) data from thread 0 (step **504**) and then read (or write as the case may be) data from thread 1 (step **510**). It is then determined whether a power off event
15 has occurred (step **512**) and if so, the process ends. If not, then the process returns to step **402**.

If it is determined that only thread 0 is active, then the latch reads (or writes) data from thread 0 (step **506**) and then continues with step **512**. If it is
20 determined that only thread 1 is active, then the latch reads (or writes) data from thread 1 (step **508**) and then continues with step **512**. Therefore, efficient use of the processor's resources is maintained by switching between the two types of multithreading. Thus, when a long
25 latency occurs in one thread, execution of the other thread is not slowed down.

The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the
30 invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art. The embodiment was chosen and described in

Docket No. AUS920000649US1

order to best explain the principles of the invention,
the practical application, and to enable others of
ordinary skill in the art to understand the invention for
various embodiments with various modifications as are
5 suited to the particular use contemplated.

11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
22